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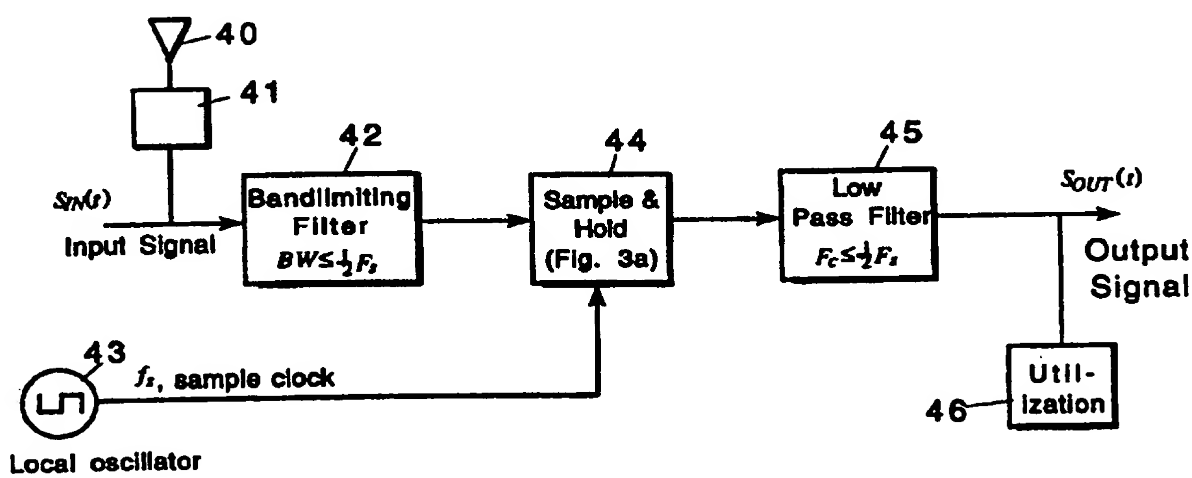

(57) Abstract

Frequency conversion is achieved in a receiver by using sample and hold (44), and track and hold for circuits in place of conventional mixers. The invention enhances spectral power efficiency usig the alias-driven frequency translation techniques and is applicable to cover IF ranges from DC to 1 GHz (with sub-Hertz resolution).

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METHOD AND APPARATUS FOR ALIAS-DRIVEN FREQUENCY DOWNCONVERSION (MIXING)

BACKGROUND AND BRIEF DESCRIPTION OF THE INVENTION:

The technique in which alternating electrical currents of different frequencies are mixed so that they modulate each other and produce, in the output components, frequencies equal to the sum and difference of the original frequencies, is called heterodyning and is traditionally achieved using a device most commonly referred to as a mixer. In modern communication systems, the mixer is a fundamental element present in many system designs. Although implementation of a traditional mixer may take one of several forms, a common feature of all traditional mixer implementations is the reliance on excitation of the mixer by a local oscillator (an alternating current source) of some fundamental frequency, f_{LO}, to achieve frequency translation of another signal by an amount equal in magnitude to f_{LO}.

Traditional frequency translation methods rely upon local oscillator frequencies equivalent to the magnitude of frequency translation desired. When using conventional mixers, it is necessary that the local oscillator frequency be equal to the magnitude of frequency translation desired. Typically, as these local oscillator frequencies become higher, circuit complexity, behavior, and electrical power consumption increase. This is especially true in oscillator implementations supporting a broad frequency tuning range and having requirements for fine frequency

tuning resolution, precision, and accuracy.

An object of the invention is to provide frequency downconversion apparatus and method which has a broad IF tuning range, enhanced spectral efficiency, and which simplifies local oscillator requirements; a further object of the invention is to provide frequency downconversion using sample-and-hold and track-and-hold circuits which have wide tuning range, low component-content and higher reliability.

The present invention provides apparatus and methods of RF frequency translation which may be termed Alias-Driven Frequency Downconversion. The invention can be implemented in part or in its entirety in analog signal-, digital signal-, and combined analog/digital signal-processing systems and is most effective when applied in translating a signal to lower frequencies (downconversion) more efficiently than existing techniques using conventional mixer technologies.

The ability to perform frequency translation of bandwidth-limited signals by integer multiples of the local oscillator frequency f_{LO} and with greater spectral power efficiency results in substantial savings in design and implementation complexity, power consumption, size, and cost with simultaneous enhancement to performance and reliability may be realized over implementations based upon traditional methods of frequency translation.

Briefly described, in place of the conventional mixer used for downconversion in RF receivers, the present invention adapts

electronic sample-and-hold and electronic track-and-hold circuits to achieve frequency translation to a lower frequency (downconversion).

The invention is applicable to IF ranges from DC to 1 GHz (with sub-Hertz) resolution) using currently available technology and with substantially no circuit modification. The same broad input bandwidth in a conventionally designed system requires a very complex and broad range frequency synthesizer whose complexity is certain to scale upwards as the range of octaves covered by the synthesizer is increased.

BRIEF DESCRIPTION OF THE DRAWINGS:

The above and other objects, advantages and features of the invention will become more apparent when considered with the following specification and accompanying drawings wherein:

FIG. 1a is a block diagram illustrating an example of a conventional high-resolution, precision variable frequency translation method using a conventional mixer;

FIG. 1b is a block diagram illustrating a variable frequency translation method using spurious frequencies output and filtered from a digitally synthesized sinusoidal oscillator and using a conventional mixer;

FIG. 2a is a block diagram of an ideal electronic sample-and-hold apparatus;

FIG. 2b illustrates the time-domain action of the ideal electronic sample-and-hold apparatus;

FIG. 2c is an illustration of the components of the frequency-domain transfer function for an ideal electronic sample-and-hold apparatus;

FIG. 3a is a block diagram of an ideal track-and-hold apparatus;

FIG. 3b illustrates the time-domain action of the ideal electronic track-and-hold apparatus;

FIG. 3c is an illustration of the frequency-domain transfer function components of an ideal electronic track-and-hold apparatus;

FIG. 4a is a block diagram illustrating frequency translation to a lower frequency (downconversion) utilizing the Alias-Driven Frequency Translation method as implemented in an apparatus using an electronic sample-and-hold device;

FIG. 4b graphically analyzes the single-sided frequency-domain donwconversion of the apparatus described in Fig. 4a;

FIG. 5a is a block diagram illustrating frequency translation to a lower frequency (downconversion) utilizing the Alias-Drive Frequency Translation method as implemented in an apparatus using an electronic track-and-hold device;

FIG. 5b graphically analyzes the single-sided frequency-domain downconversion of the apparatus described in Fig. 5a;

FIG. 6a illustrates an architecture and apparatus for Alias-Driven Frequency Downconversion utilizing an electronic sample-and-hold apparatus;

FIGS. 6b through 6g graphically analyze in the time domain and frequency domain the signal, f_{in}, as it progresses through the system presented in Fig. 6a at the three test points labeled TP4 through TP6;

FIGS. 7a and 7b compare the spectral power efficiency of frequency downconversion approaches using the ideal conventional mixer implementation of Fig. 1a or 1b and of the Alias-Driven Frequency Translation implementation using an electronic sample-and-hold apparatus as illustrated in Fig. 6a;

FIG. 8a illustrates an architecture and apparatus for Alias-Driven Frequency Downconversion utilizing an electronic track-and-hold apparatus;

FIG. 8b through 8g graphically analyze in the time domain and frequency domain the signal, f_{in}, as it progresses through the system presented in Fig. 8a at the three test points labeled TP7 through TP9;

FIG. 9 compares the spectral power efficiency of frequency donwconversion approaches using the ideal conventional mixer implementation of Fig. 1a or 1b and of the Alias-Driven Frequency Translation implementation using an electronic track-and-hold apparatus as illustrated in Fig. 8a.

DETAILED DESCRIPTION OF THE INVENTION:

Referring to Fig. 1a, a conventional high resolution, precision variable frequency translation method is disclosed wherein the input F_{IF} signal is applied through an image reject

filter 10 to a conventional mixer 11. A frequency control word F_{NCO} is applied along with the clock frequency F_{CLK} to a number controlled oscillator (NCO) 12, the output of which is converted to an analog signal in digital-to-analog converter 13, low pass filtered by low pass filter (LPF) 14 and supplied as the signal from the numerically controlled oscillator F_{NCO} to a conventional mixer 15. A fixed frequency oscillator 16 supplies a second input to mixer 15 and the output is filtered by bandpass filter 17 so that the output $F_{NCO} + F_{LO}$ is applied as a second input to mixer 11. The output from mixer 11 is passed through bandpass filter 18 as the downconverted signal $F_{IF} - (F_{NCO} + F_{LO})$.

Fig. 1b is a block diagram illustrating a variable frequency translation method using spurious frequency outputs and filtered from a digitally synthesized sinusoidal oscillator and using a conventional mixer. In this system the signal from the numerically controlled oscillator 12′ is converted to an analog signal in a high performance digital/analog converter 13′ and the signal is filtered in bandpass filter 17′ and the resulting output F_{CLK} +/- F_{NCO} is supplied through a high frequency amplifier 19 and applied as a second input to the conventional mixer 11′.

Fig. 2a is a block diagram illustrating an ideal electronic sample and hold apparatus wherein the analog input signal V_N (see Fig. 2b) is applied through an amplifier 20 which has a gain of 1 to electronic sampler switch 21 which is operated by an impulse generator 22 having a sample timing clock F_{CLK} (see Fig. 2b, top line). The sampled pulses from switch 21 are stored in a storage

device, such as capacitor 22 and provided as an analog output through amplifier 23 which has a gain of 1. Fig. 2c (line 1) is a simplified diagram of the ideal electronic sample and hold apparatus shown in Fig. 2a. Fig. 2c (line 2) illustrates an ideal sampler transfer function for the sampler shown in Fig. 2c, (line 1). Fig. 2c (line 3) illustrates a zero-order hold transfer function for the circuit shown in Fig. 2c (line 1).

Fig. 3a is a block diagram of an ideal track-and-hold circuit in which an analog input signal V_{IN} is amplified by amplifier 30 (which has a gain of 1) and output is sampled by electronic sampling switch 31, which receives track/hold switch control signals from source 32. The output is stored on charge storage capacitor 33, passed through amplifier 34. Fig. 3b (line 1) shows the track (complement) and hold time intervals "T" and "H" which have a time period T_s. Fig. 3b (line 2) shows the time domain action of the track-and-hold apparatus of Fig. 3a. The input analog signal V_{IN} is shown as a sinusoidal wave (light trace) and the analog output V_{OUT} (heavy trace) tracks the input signal during the track periods (T) and holds the last value during the hold periods (H). Thus, at 35-1 the output trades the portion of the sine wave during track period T_1 and holds the last valve 35-2 during period H_2. During track period T_2 the signal tracks the sine wave at 35-3 and holds the last value 35-4, etc.

Fig. 3c (line 1) illustrates the frequency domain transfer function components of an electronic track-and-hold circuit and

lines 2-4 illustrate the sampler transfer function (line 2), the hold transfer function (line 3) when $T_H \leq T_3$ and the track transfer function (line 4) when T_T is less than T_S.

Referring to the system shown in Fig. 4, the signal on antenna 40 is amplified by broad-band amplifier 41 and its output $S_{IN}(\tau)$ is applied as the input signal to band-limiting filter 42 which has a bandwidth equal to or less than 1/2 the sampling frequency f_s of local oscillator 43 (which in this embodiment is a square wave source). Sampling clock signals f_s from source 43 are applied to sample-and-hold circuit 44 (which ha the form shown in Fig. 2a). The output of sample-and-hold circuit 44 is filtered by low pass filter 45 which has a center frequency which is about 1/2 of the sampler clock frequency f_s, and the filtered output is supplied to a utilization device 46 for further processing. Low order aliases 47 and higher order aliases 48 are shown in Fig. 4b (line 2) (before low pas filter 45) and the output signal to the utilization device 46 is shown in Fig. 4b (line 3).

Fig. 5a shows a receiver system similar to Fig. 4a but using a track-and-hold circuit 50 for producing the alias-driven frequency translation. In Fig. 5b (lines 1-4), graphically illustrates the single-sided frequency f_a while Fig. 5 (line 2) illustrate the spectral output prior to the low pass filter 45' hold function (T_H hold time); Fig. 5 (line 3) shows the spectral output (prior to low pass filter 41) track function τ = track time, and Fig. 5 (line 4) shows the spectral output signal S_{OUT}

(f).

Fig. 6a shows the architecture for the alias-driven downconversion system of this invention using the sample-and-hold system described earlier, and Figs. 6b through 6g illustrate time and frequency domain aspects of the signal at test points TP_4, TP_5 and TP_6.

Figs. 7a and 7b provide graphical comparisons of spectrals of the system of Fig. 1a, 1b (test point 3) with system of the present invention (test points in Fig. 6a).

Fig. 8a shows the architecture for the alias-driven downconversion system of this invention using the electronic track-and-hold system described earlier herein with the waveform at test points TP_7, TP_8 and TP_9 being illustrated in figs. 8b through 8g.

Finally, Fig. 9 compares the spectral efficiency of frequency downconversion of the present invention with conventional mixer systems of the prior art.

ADVANTAGES OF THE INVENTION:

Traditional frequency translation methods rely upon local oscillator frequencies equivalent to the magnitude of frequency translation desired. When using conventional mixers, it is necessary that the local oscillator frequency be equal to the magnitude of frequency translation desired. Typically, as these local oscillator frequencies become higher, circuit complexity, behavior, and electrical power consumption increase. This is especially true in oscillator implementations supporting a broad

frequency tuning range and having requirements for fine frequency tuning resolution, precision, and accuracy. In simplifying local oscillator requirements, the method of Alias-Driven Translatio. of this invention offers several distinct advantages over the conventional method. These advantages are:

Simplified tunable high resolution local oscillator design.

Figs. 1a and 1b illustrate conventional approaches to high-resolution, precision tunable frequency translation. In the architecture of Fig. 1a, high-resolution, precision, and tunability are achieved using a numerically controlled oscillator. Since the tunable range of a numerically controlled oscillator (NCO) implemented as in Fig. 1a is restricted to frequencies below $0.5*_{clk}$ (theoretical Nyquist limit) and approximately $0.4*_{clk}$ (practical implementation limit), where F_{clk} represents the clock rate of the NCO and which itself has practical limitations, the NCO output is frequently augmented by heterodyning with a precision oscillator in order to shift the tunable range of the numerically controlled oscillator into usable range of local oscillator requirements. Using this approach for frequency translation provides a frequency tuning bandwidth restricted to the lesser of the tuning range of the NCO, and the filter bandwidth of Filter-B. Disadvantages of this implementation architecture include: narrow tuning range, high component count, and lowered reliability.

Fig. 1b illustrates an approach to synthesizing high-resolution, precision frequencies for local oscillator

implementation by selectively bandpass filtering for a high order frequency spur generated by a numerically controlled oscillator at the output of a digital-to-analog converter. Using this method for frequency translation provides a frequency tuning bandwidth restricted to the lesser of the tuning range of the NCO and the filter bandwidth of the bandpass reconstruction filter, Filter-A. Because of the amplitude degradation associated with higher order spurious response out of the NCO, it is often necessary to provide signal amplification to the selected frequency spur. Disadvantages of this implementation architecture include: a narrow tuning range restricted by the need for a bandpass reconstruction filter, increased local oscillator phase noise and the increased power consumption necessary to support the high frequency amplifiers (both due to the degraded amplitude of the selected frequency spur), and the need for a high-performance digital-to-analog converter featuring the high output slew rates and fast settling time necessary to generate the desired high frequency spurious response and to suppress undesired frequency spur generation.

As described above and illustrated in the drawings, downconversion according to this invention provide a broad IF tuning range with enhanced spectral power efficiency.

The invention has a broad input signal range resulting in circuit simplification compared to conventional approaches when building a system with equivalent functionality. For example, the invention can be used to cover IF ranges from DC to 1 GHz

(with sub-Hertz resolution) using currently available technology and with substantially no circuit modification.

While preferred embodiments of the invention have been described and illustrated, it will be appreciated that other embodiments, adaptations and modifications of the invention will be readily apparent to those skilled in the art.

WHAT IS CLAIMED IS:

CLAIMS

1. In a receiver system having an antenna RF amplifier coupled to said antenna for receiving intelligence modulated RF signals and producing a received intelligence modulated (RIM) RF signal and means for downconverting said RIM RF signal for use by a utilization circuit, the improvement in said means for downconverting comprising:

first filter means connected to receive said RIM RF signal and having a first filter output,

aliasing circuit means including electronic switch means connected to said first filter output, and a storage means connected to said switch means, means for producing signal, and switch control signal means for applying a control signal f_s to said electronic switch to connect and disconnect said RIM RF signal to said storage means,

a low pass filter means having a center frequency fc $\leq$ 1/2 Fs connected to said storage means, and

means connecting said low pass filter means to said utilization circuit.

2. The receiver system defined in claim 1 wherein said aliasing circuit means is a sample-and-hold circuit.

3. The receiver system defined in claim 1 wherein said aliasing circuit means is a track-and-hold circuit.

4. In a receiver system having an antenna RF amplifier coupled to said antenna for receiving intelligence modulated RF signals and producing a received intelligence modulated (RIM) RF signal and means for downconverting said RIM RF signal for use by a utilization circuit, the improvement in said method for downconverting comprising:

enhancing spectral power efficiency using alias-driven frequency translation of received intelligence modulated RF signals, and low pass filtering the aliased signal.

5. The invention defined in claim 4 wherein the downconversion is in the IF ranges from DC to 1 GHz (with sub-Hertz) resolution).

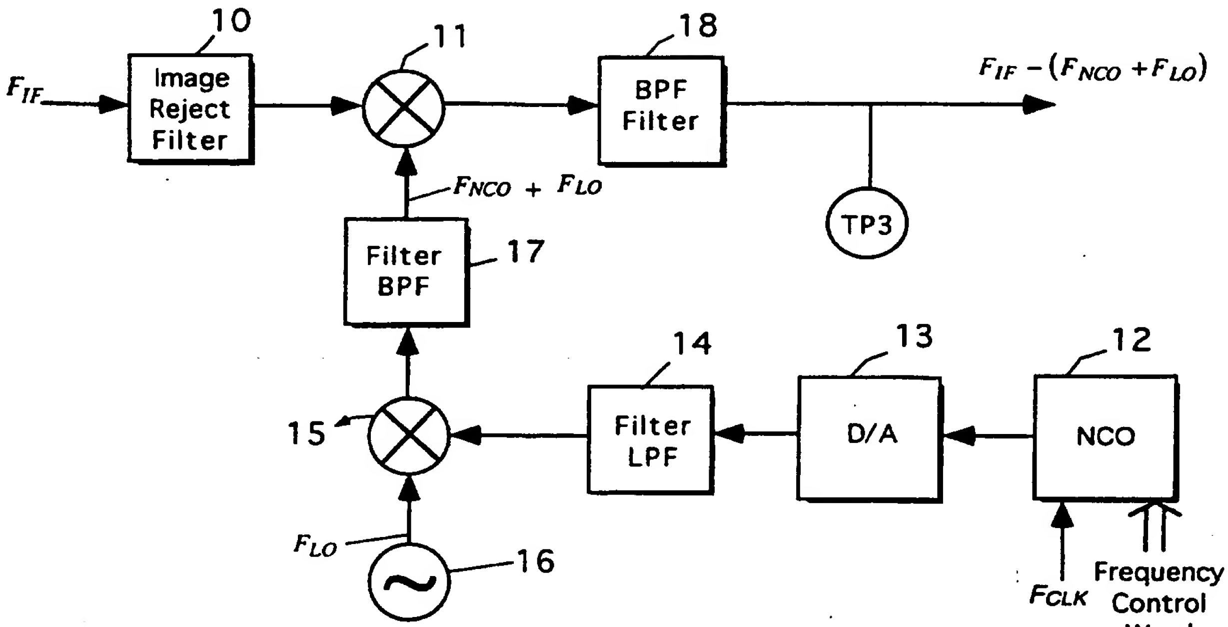


FIGURE 1a (PRIOR ART)

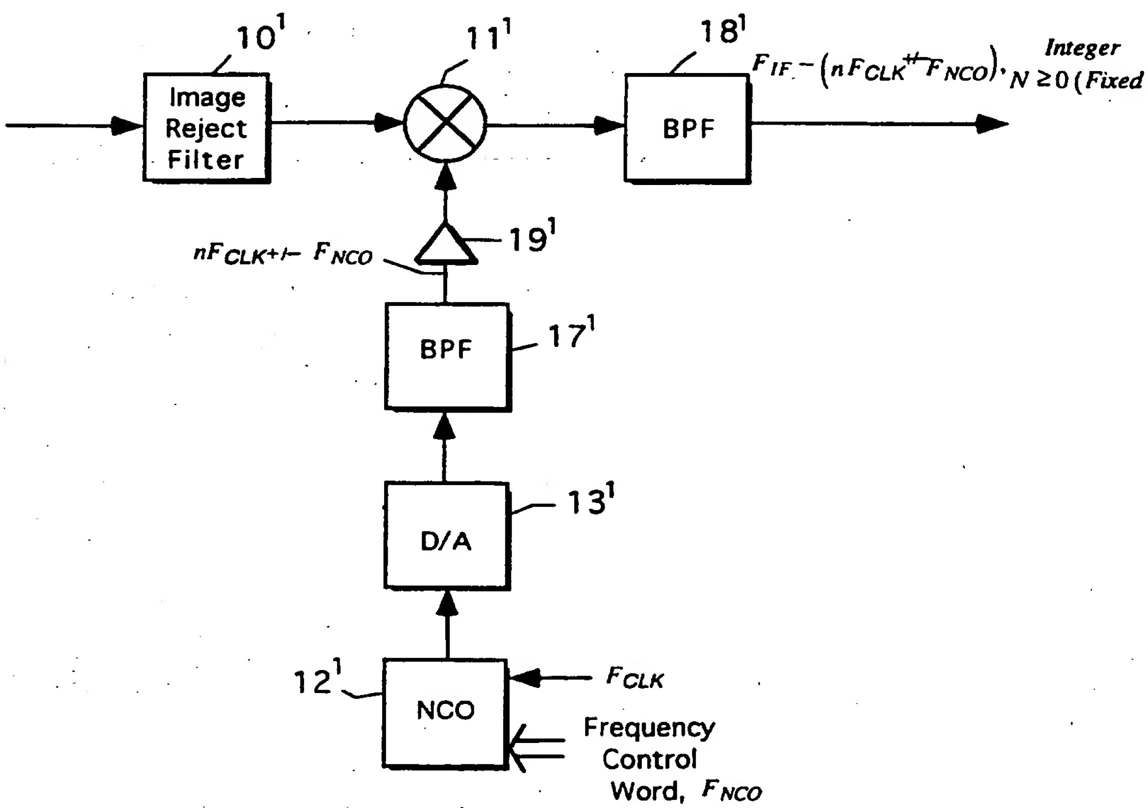


FIGURE 1b (PRIOR ART)

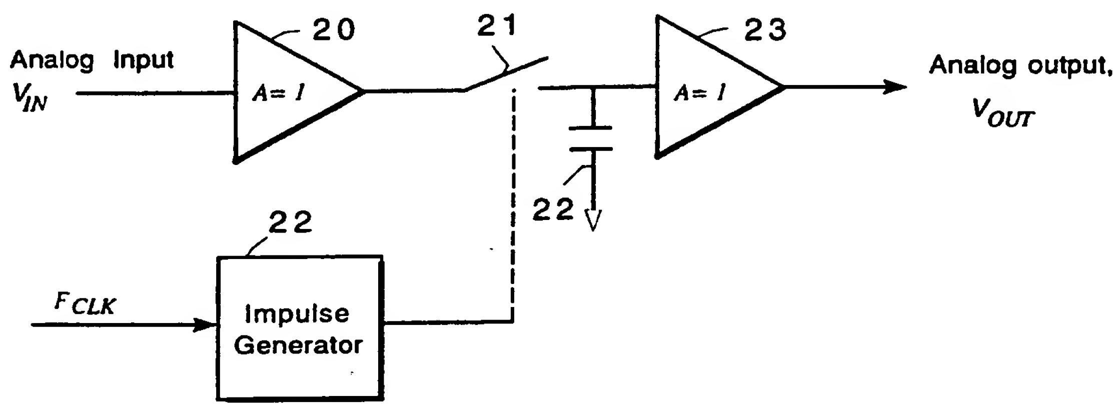


FIGURE 2a

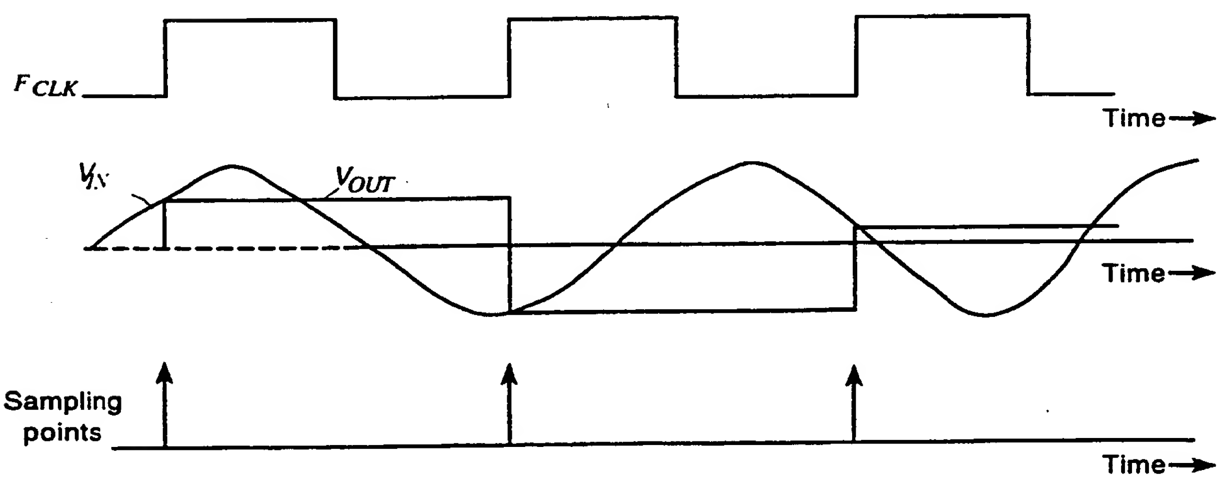


FIGURE 2b

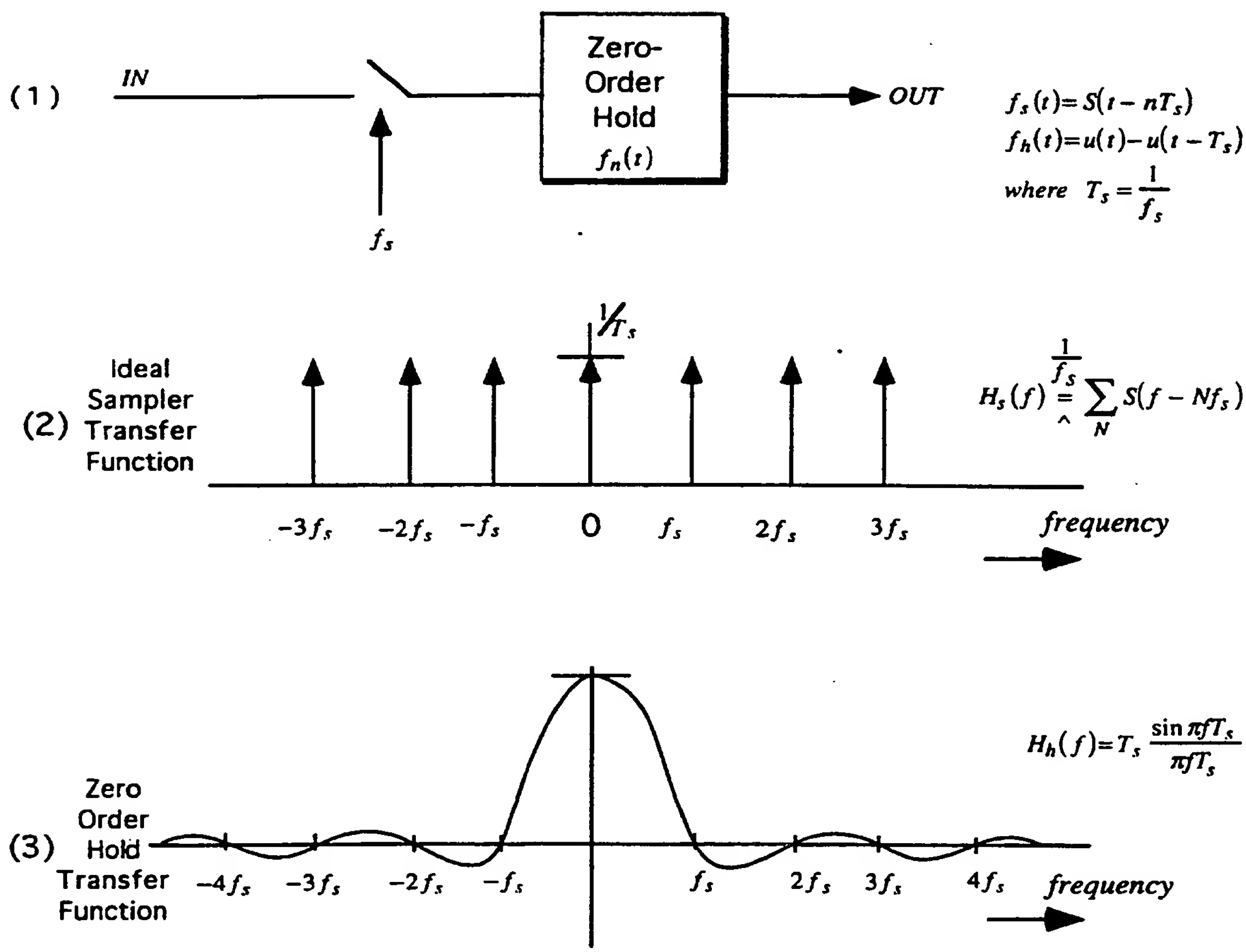

(1)
IN
Zero-Order Hold
$f_n(t)$
OUT
f_s
$f_s(t)=S(t-nT_s)$
$f_h(t)=u(t)-u(t-T_s)$
where $T_s=\frac{1}{f_s}$
(2) Ideal Sampler Transfer Function
$1/T_s$
$H_s(f) = \frac{1}{f_s}\sum_N S(f-Nf_s)$
$-3f_s$ $-2f_s$ $-f_s$ 0 f_s $2f_s$ $3f_s$
frequency
(3) Zero Order Hold Transfer Function
$H_h(f)=T_s\frac{\sin \pi f T_s}{\pi f T_s}$
$-4f_s$ $-3f_s$ $-2f_s$ $-f_s$ f_s $2f_s$ $3f_s$ $4f_s$
frequency

FIGURE 2c

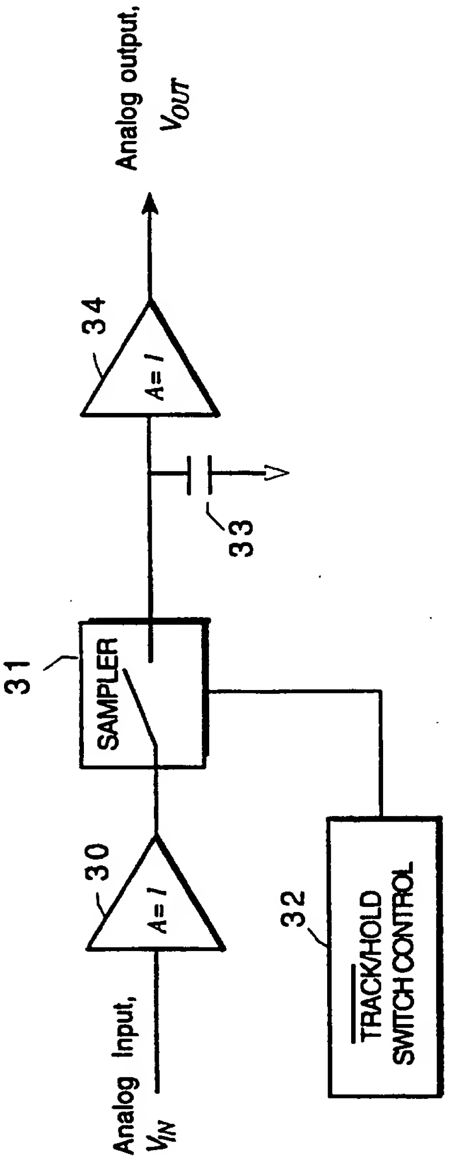


FIGURE 3a

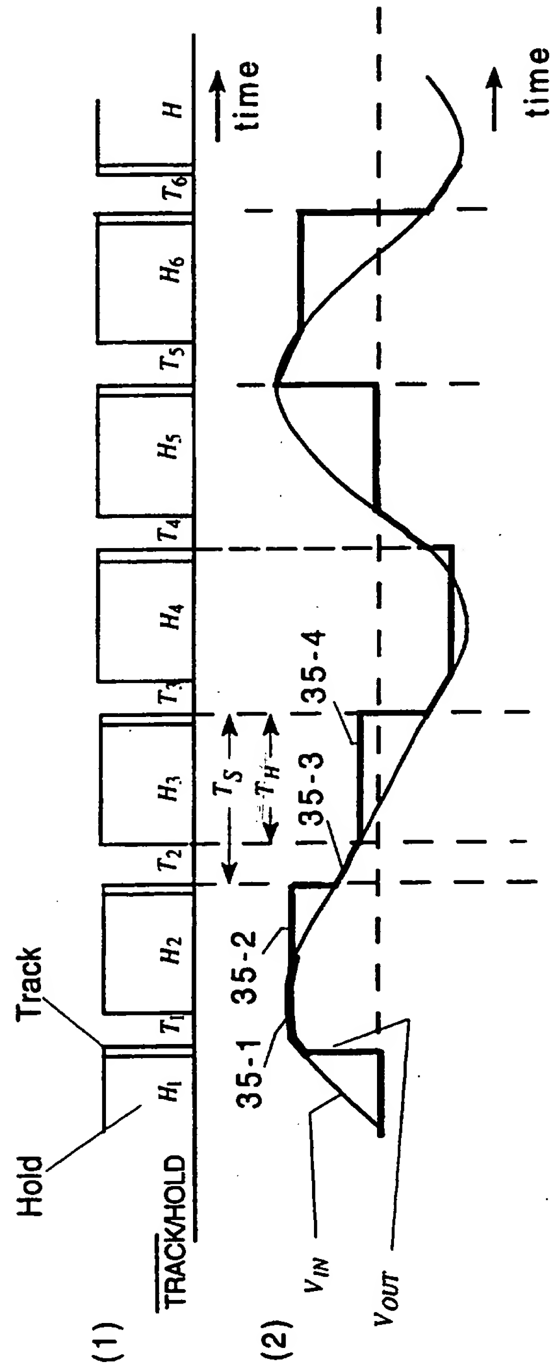


FIGURE 3b

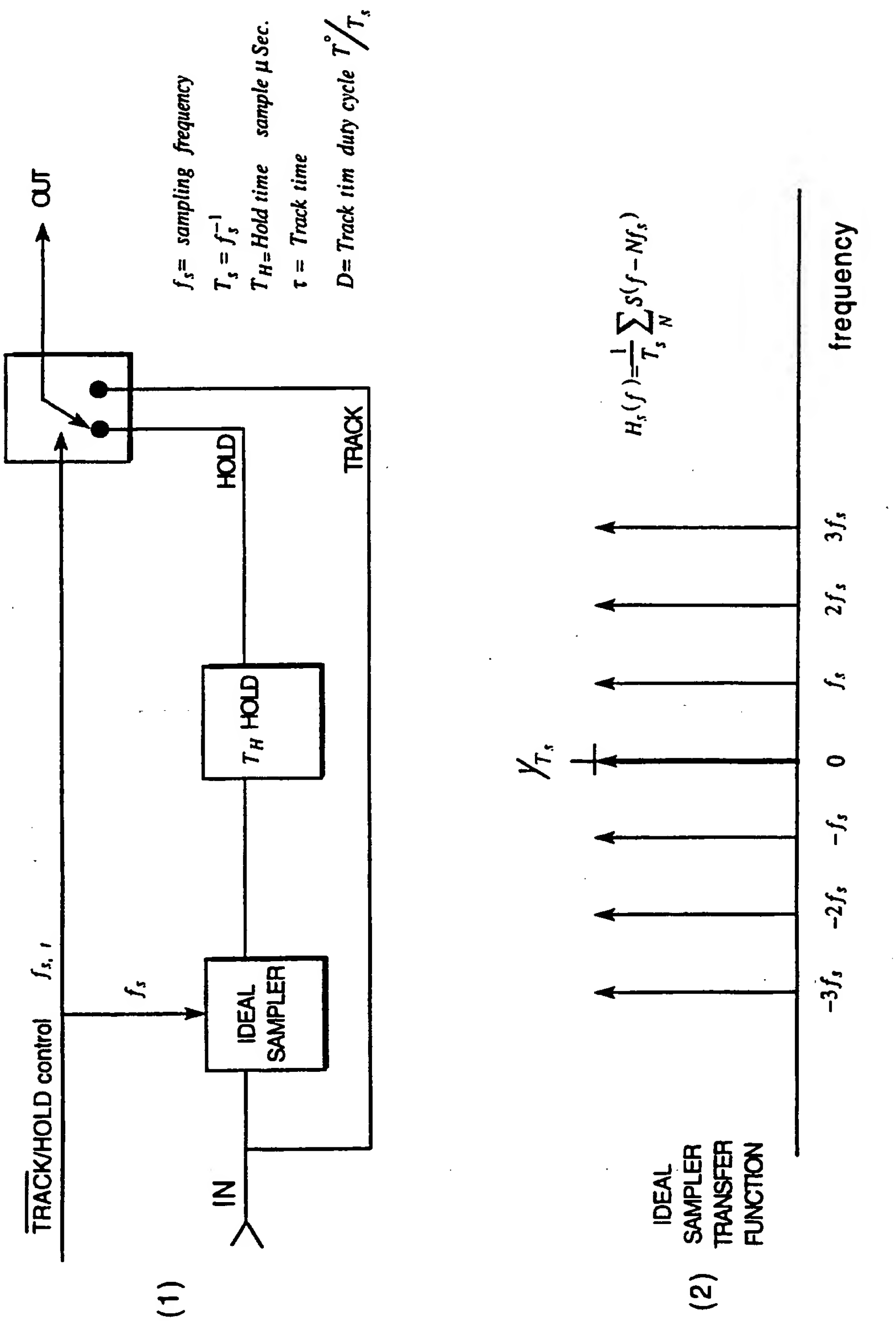


FIGURE 3C
Page 1

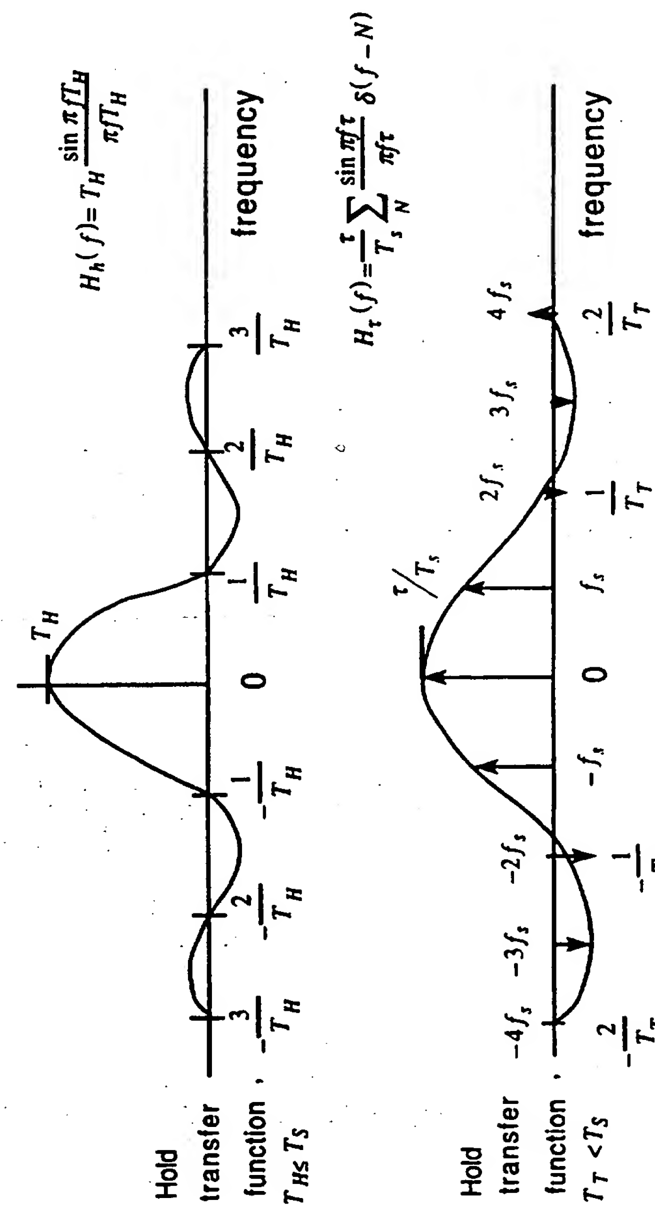


FIGURE 3C
Page 2

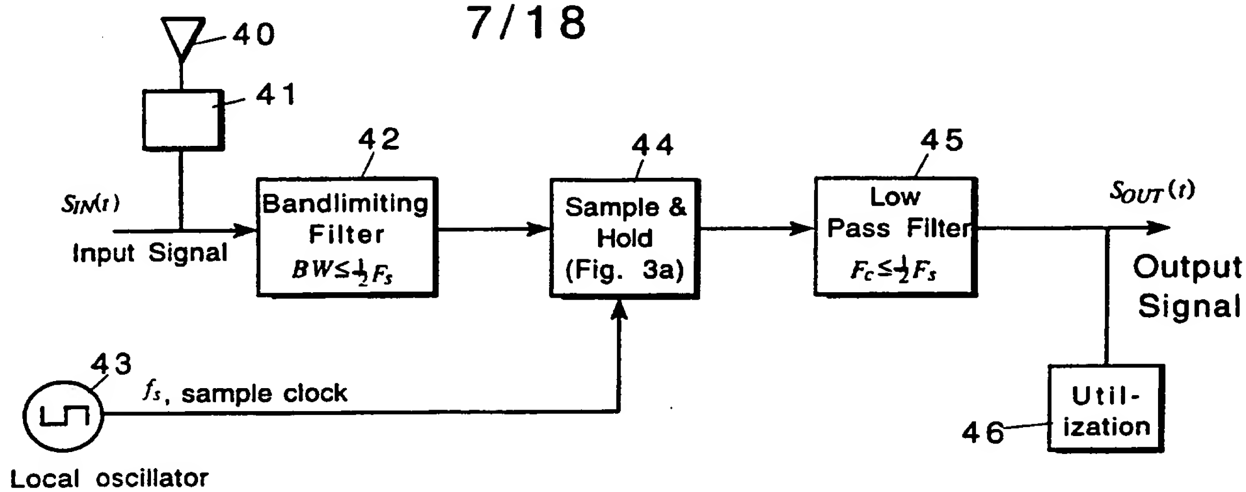


FIGURE 4a

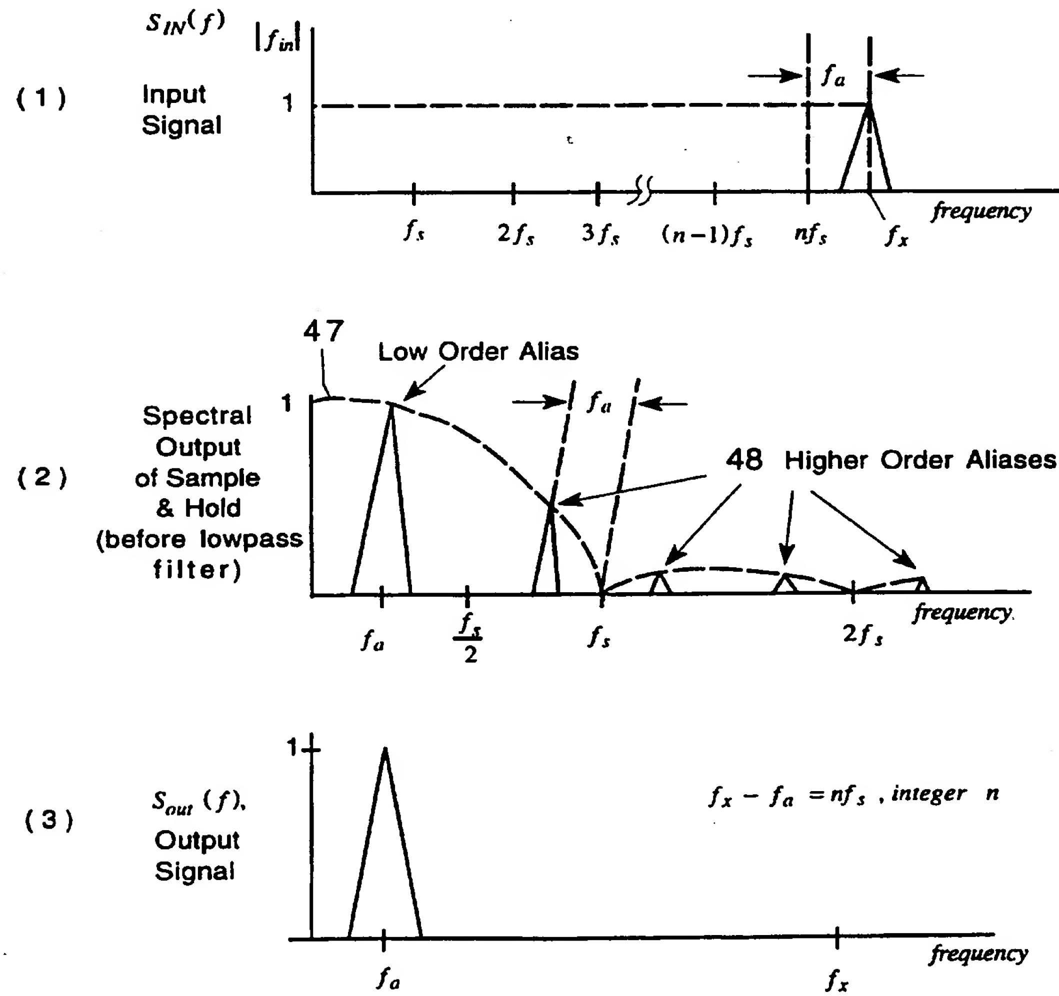
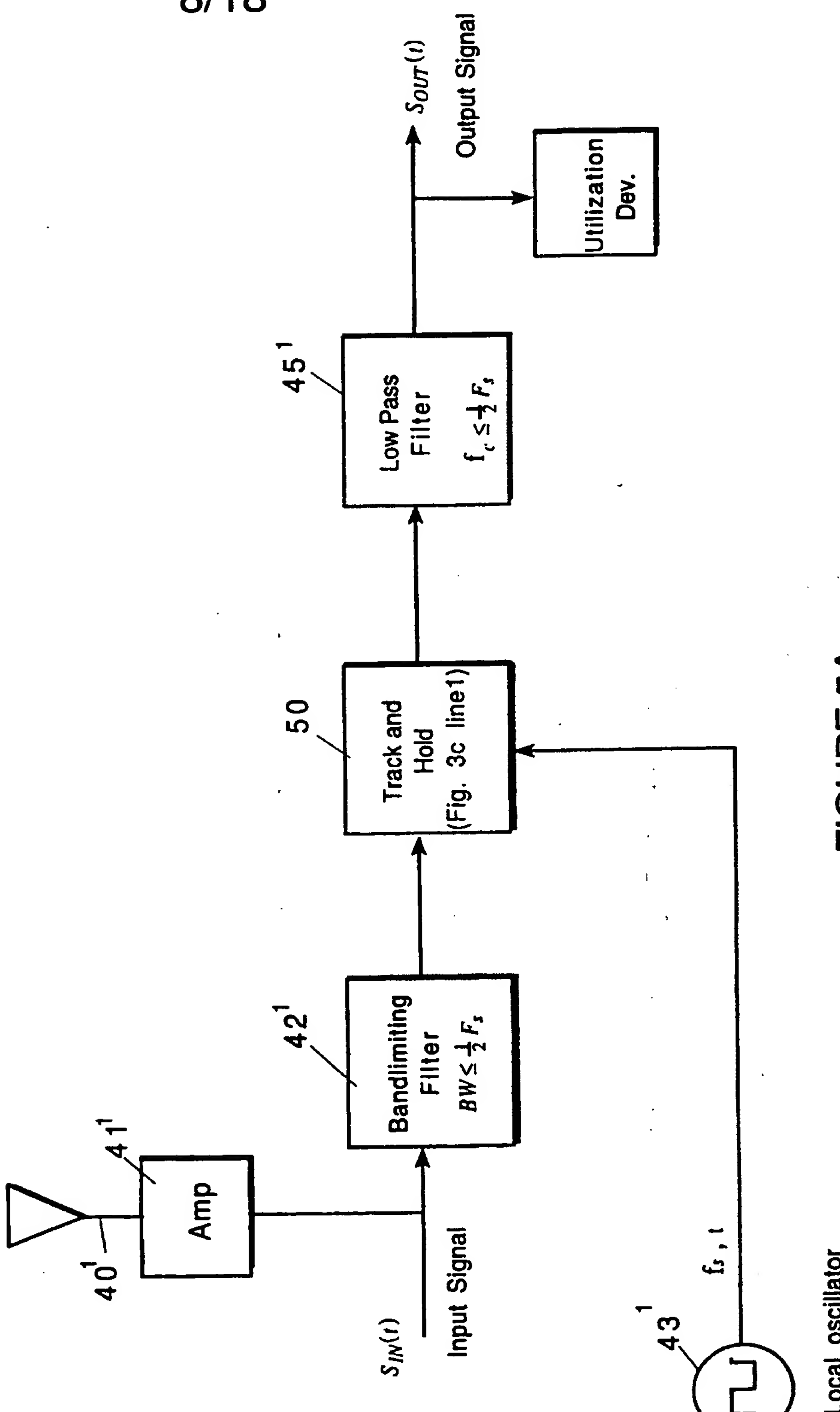
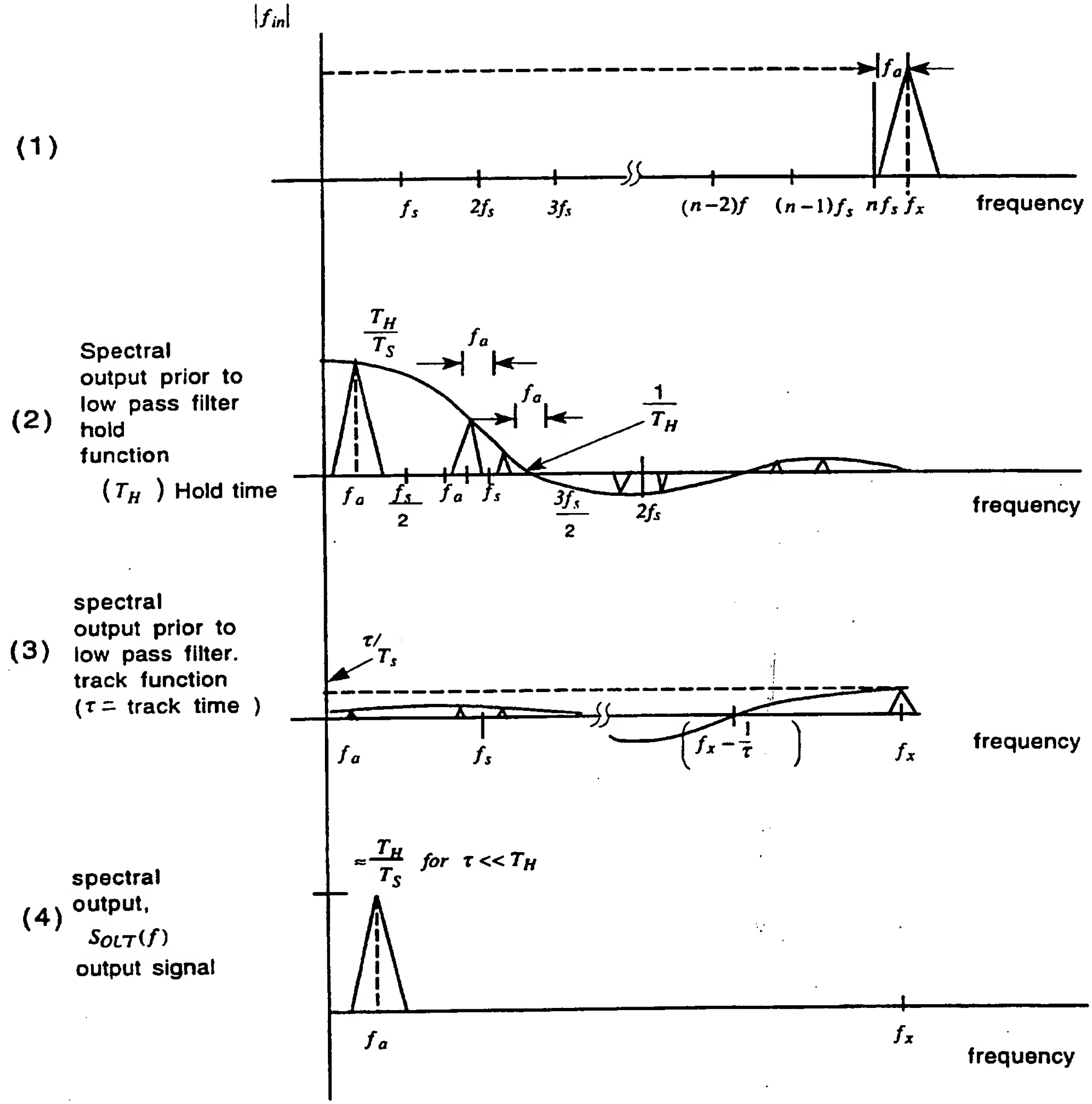


FIGURE 4b



$S_{OUT}(t)$
Output Signal
Utilization Dev.
45[1]
Low Pass Filter
$f_c \leq \frac{1}{2} F_s$
50
Track and Hold
(Fig. 3c line1)
42[1]
Bandlimiting Filter
$BW \leq \frac{1}{2} F_s$
41[1]
Amp
40[1]
$S_{IN}(t)$
Input Signal
f_s, t
43[1]
Local oscillator

FIGURE 5A



$|f_{in}|$
(1)
f_a
f_s
$2f_s$
$3f_s$
$(n-2)f$
$(n-1)f_s$
nf_s
f_x
frequency
(2)
Spectral output prior to low pass filter hold function
(T_H) Hold time
$\frac{T_H}{T_S}$
f_a
$\frac{1}{T_H}$
f_a
$\frac{f_s}{2}$
f_a
f_s
$\frac{3f_s}{2}$
$2f_s$
frequency
(3)
spectral output prior to low pass filter. track function
(τ = track time)
τ/T_s
f_a
f_s
$\left(f_x - \frac{1}{\tau}\right)$
f_x
frequency
(4)
spectral output, $S_{OLT}(f)$ output signal
$\approx \frac{T_H}{T_S}$ for $\tau << T_H$
f_a
f_x
frequency

FIGURE 5B

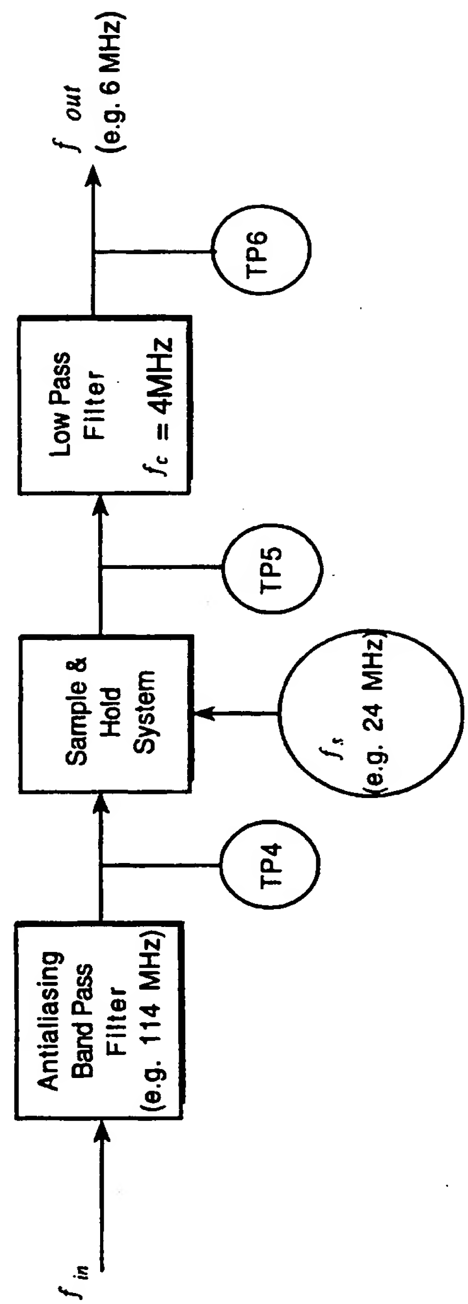

f_{in}
Antialiasing Band Pass Filter (e.g. 114 MHz)
TP4
Sample & Hold System
f_s (e.g. 24 MHz)
TP5
Low Pass Filter f_c = 4MHz
TP6
f_{out} (e.g. 6 MHz)

FIGURE 6A

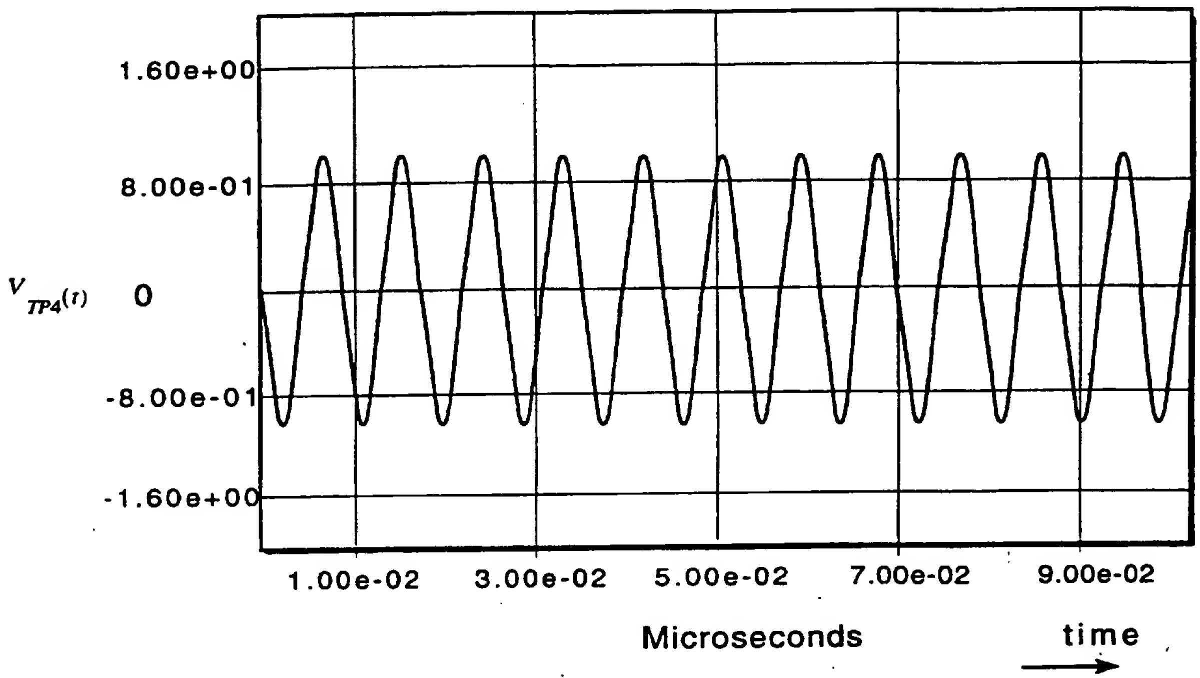


FIGURE 6B

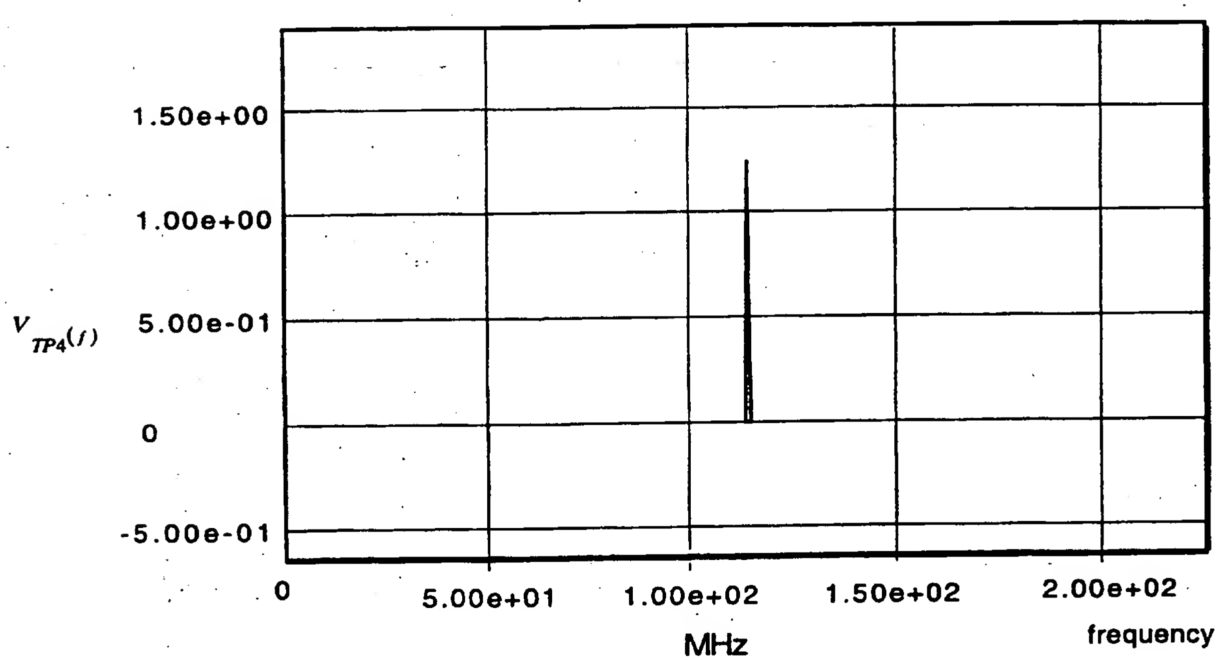


FIGURE 6C

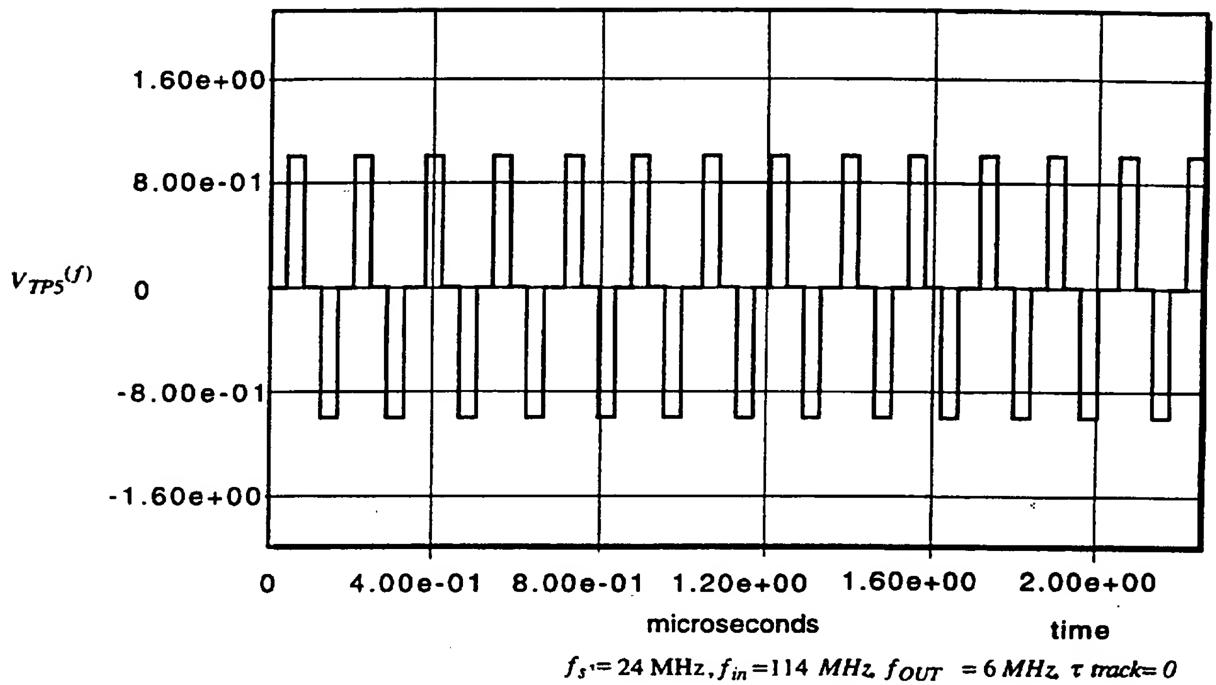


FIGURE 6D

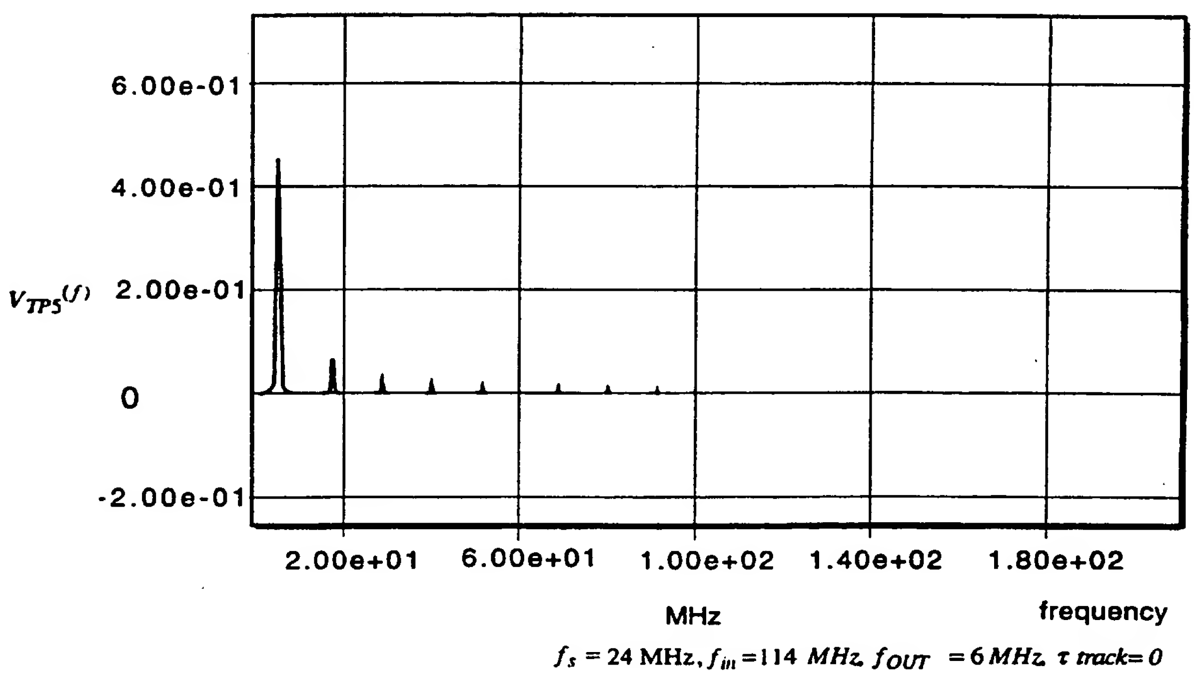
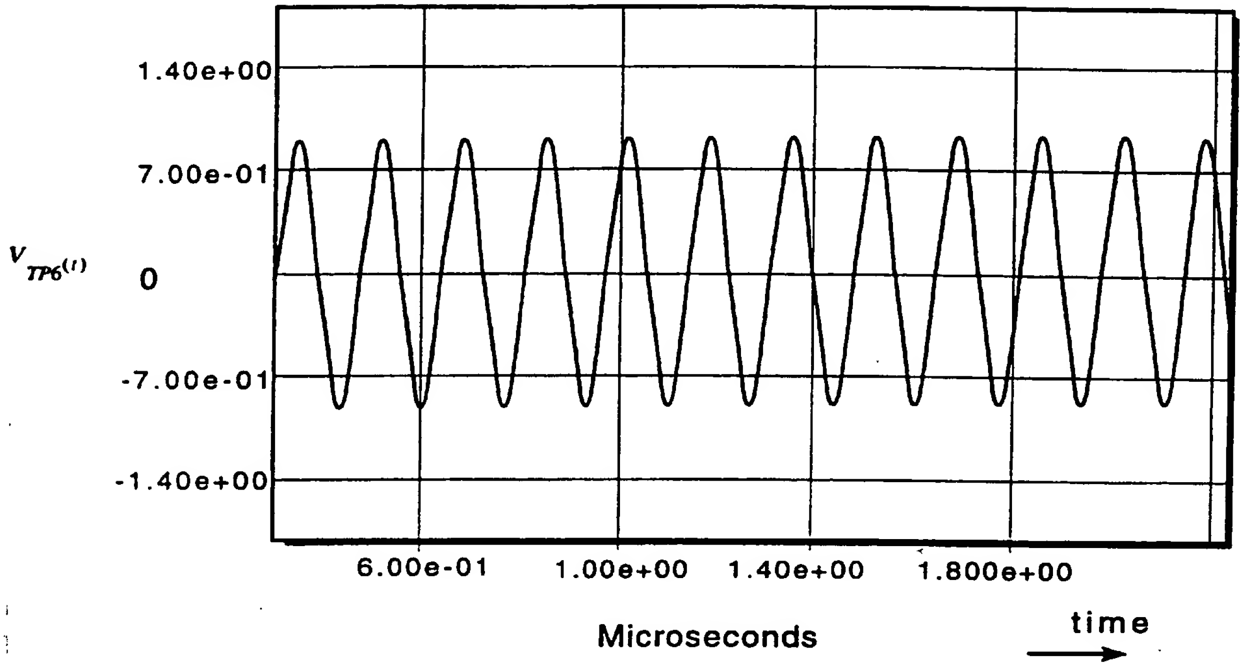
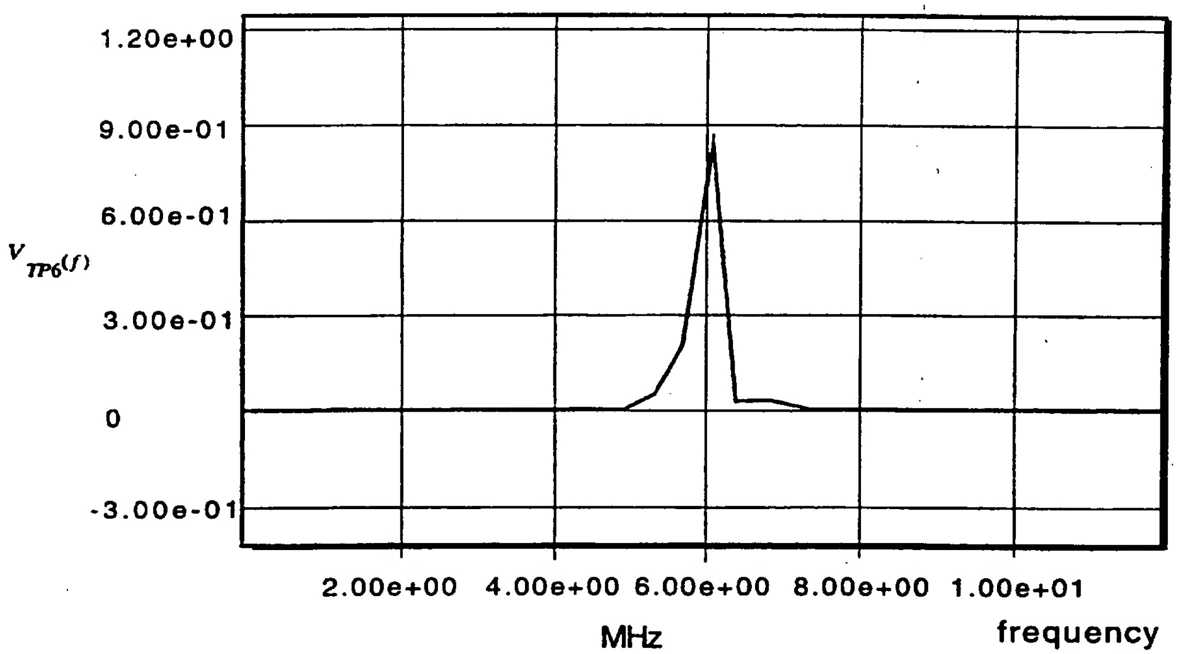


FIGURE 6E



$f_s = 24\,MHz, f_{in} = 114\ MHz,\ f_{OUT}\ = 6\,MHz,\ \tau\ track = 0$

FIGURE 6F



$f_s = 24\,MHz, f_{in} = 114\ MHz,\ f_{OUT}\ = 6\,MHz,\ \tau\ track = 0$

FIGURE 6G

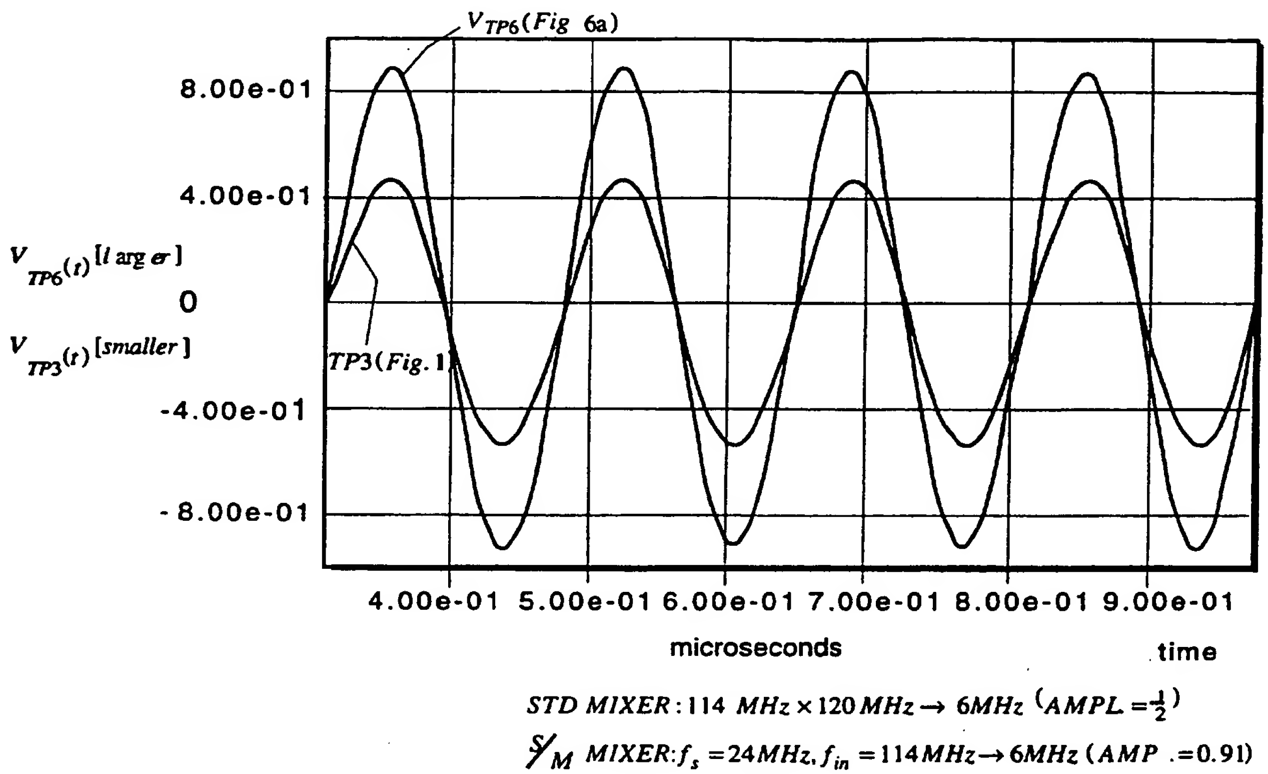


FIGURE 7A

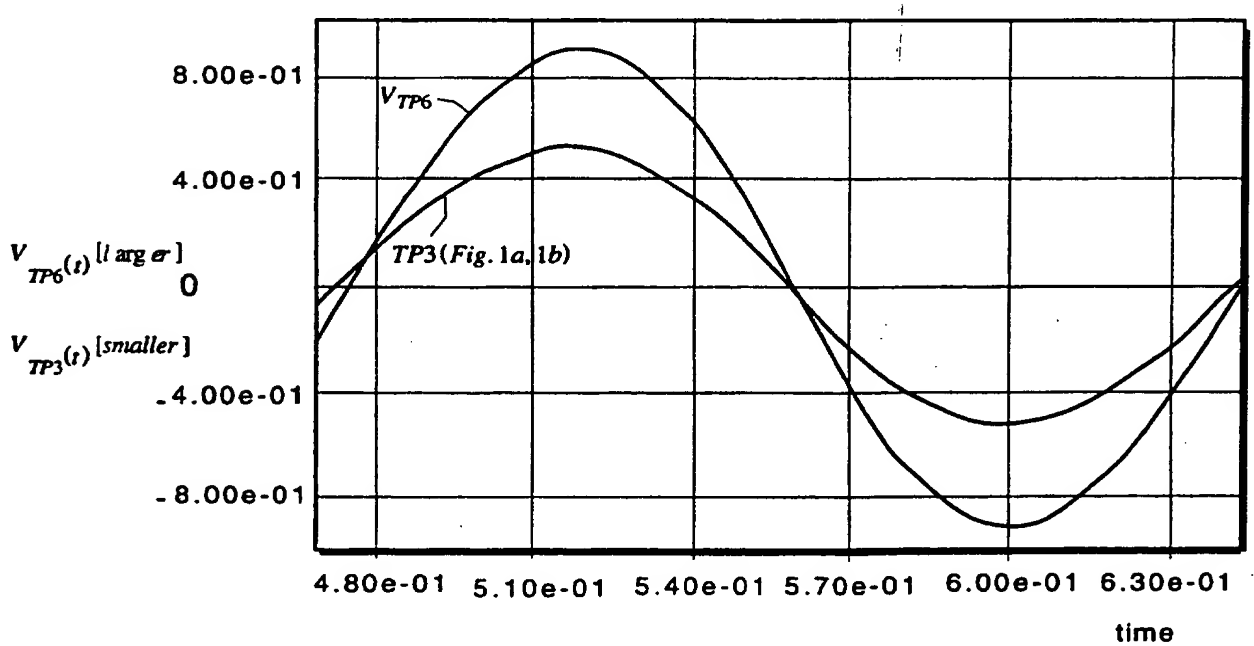


FIGURE 7B

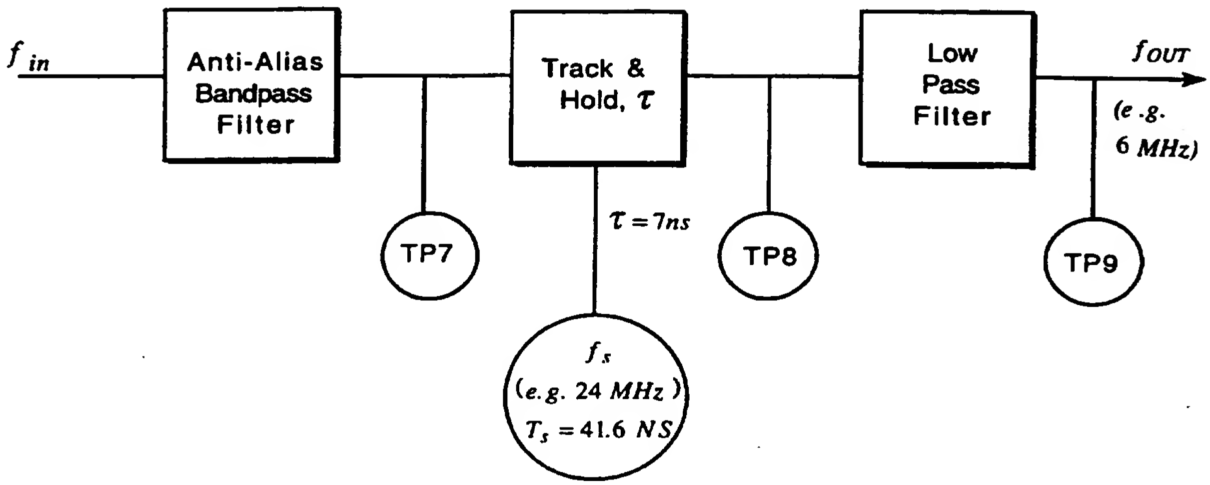
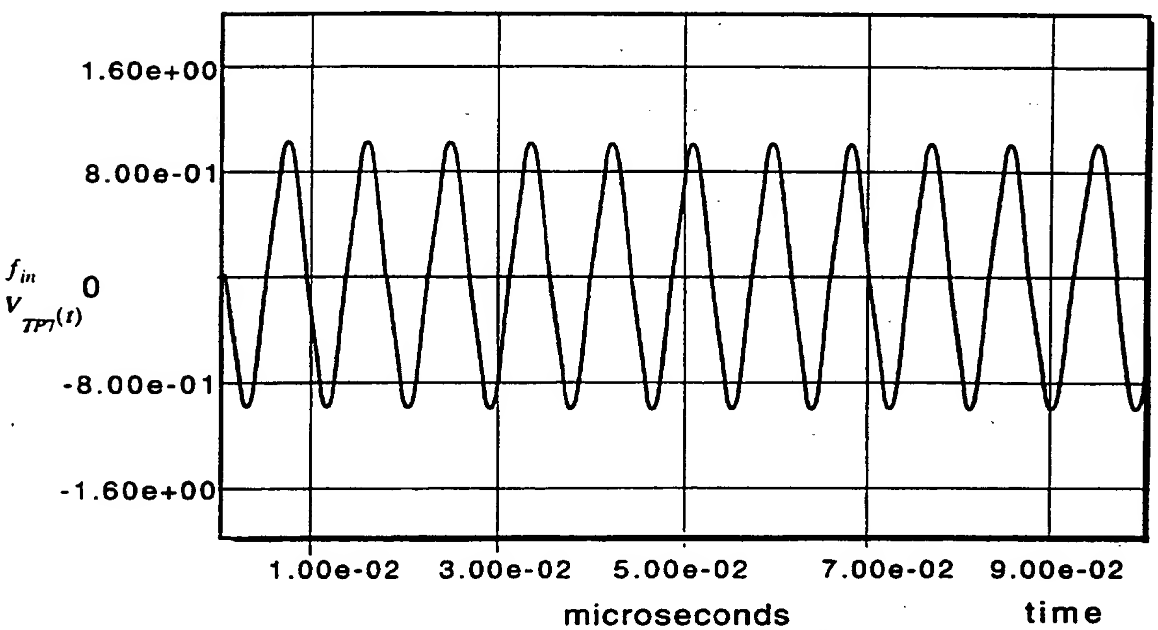


FIGURE 8A



$f_s = 24\ MHz,\ f_{in} = 114\ MHz,\ f_{OUT} = 6\ MHz,\ \tau\ track = 7_{ns}$

FIGURE 8B

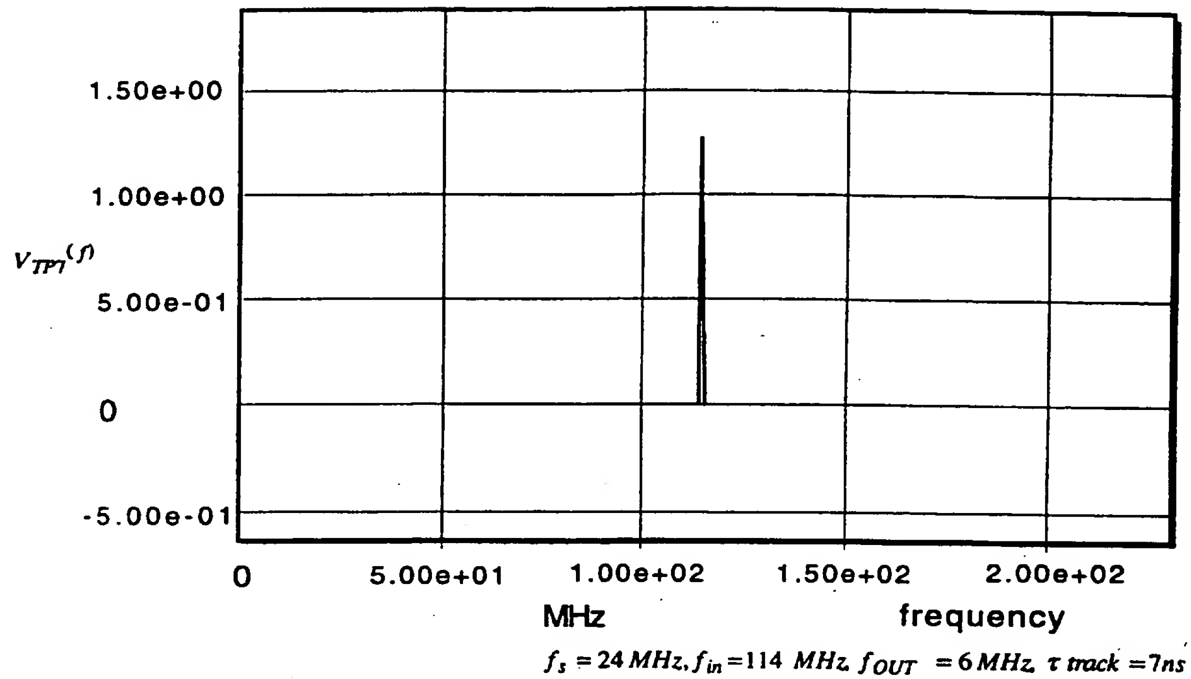


FIGURE 8C

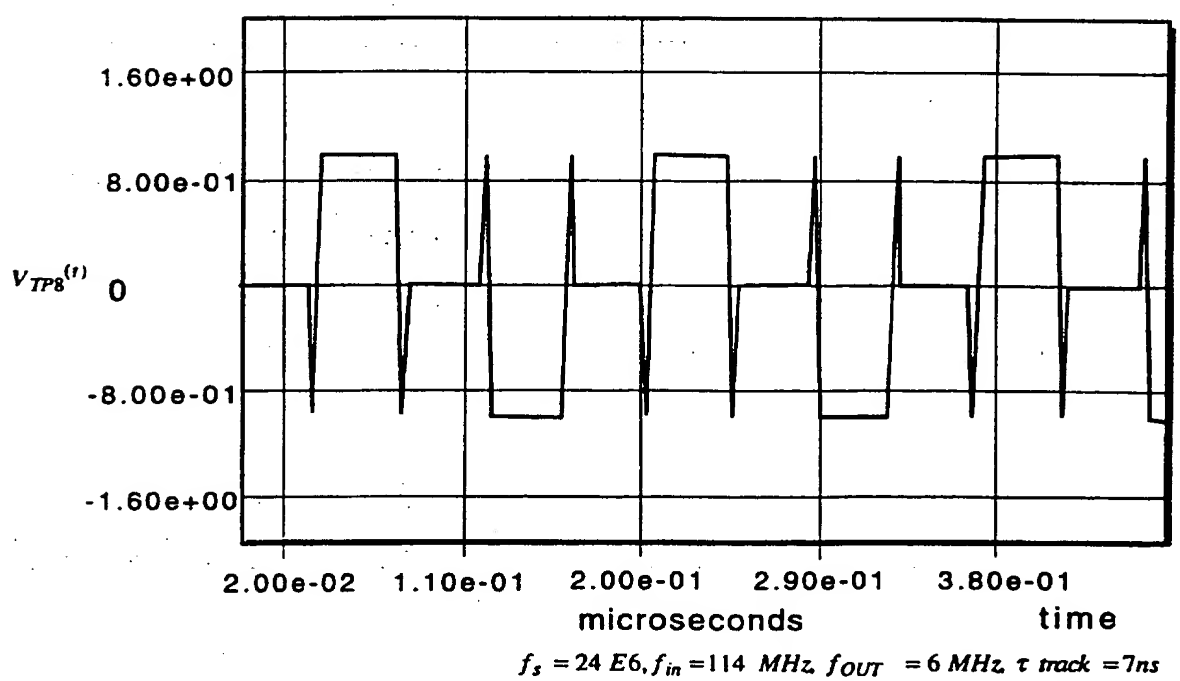
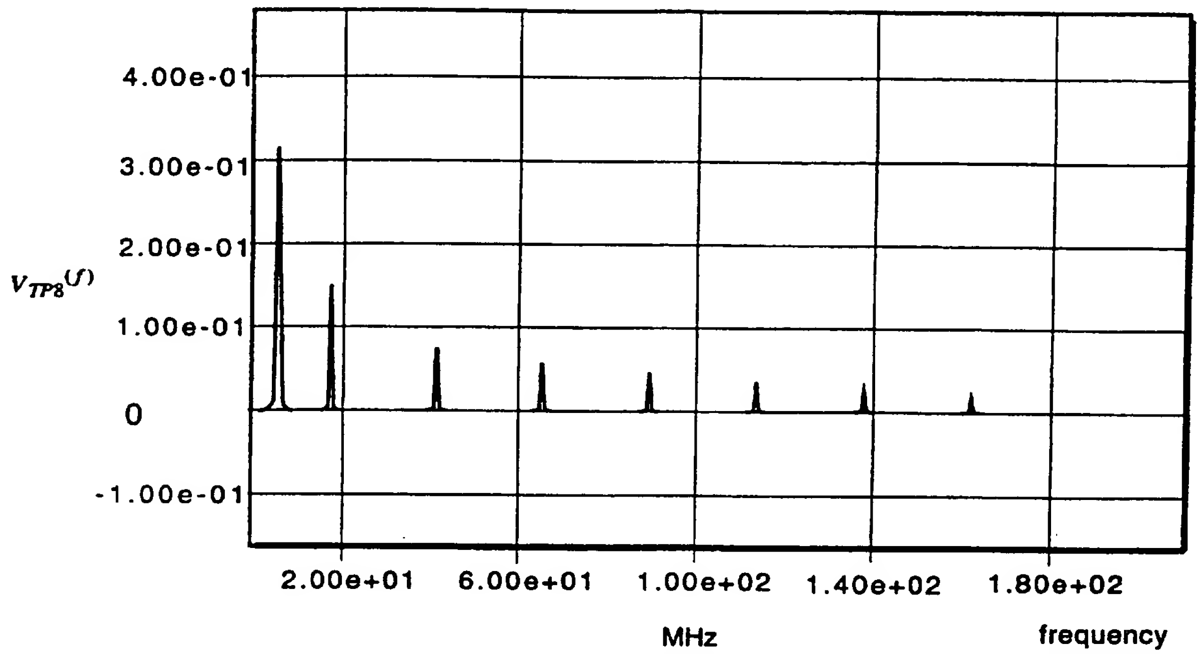
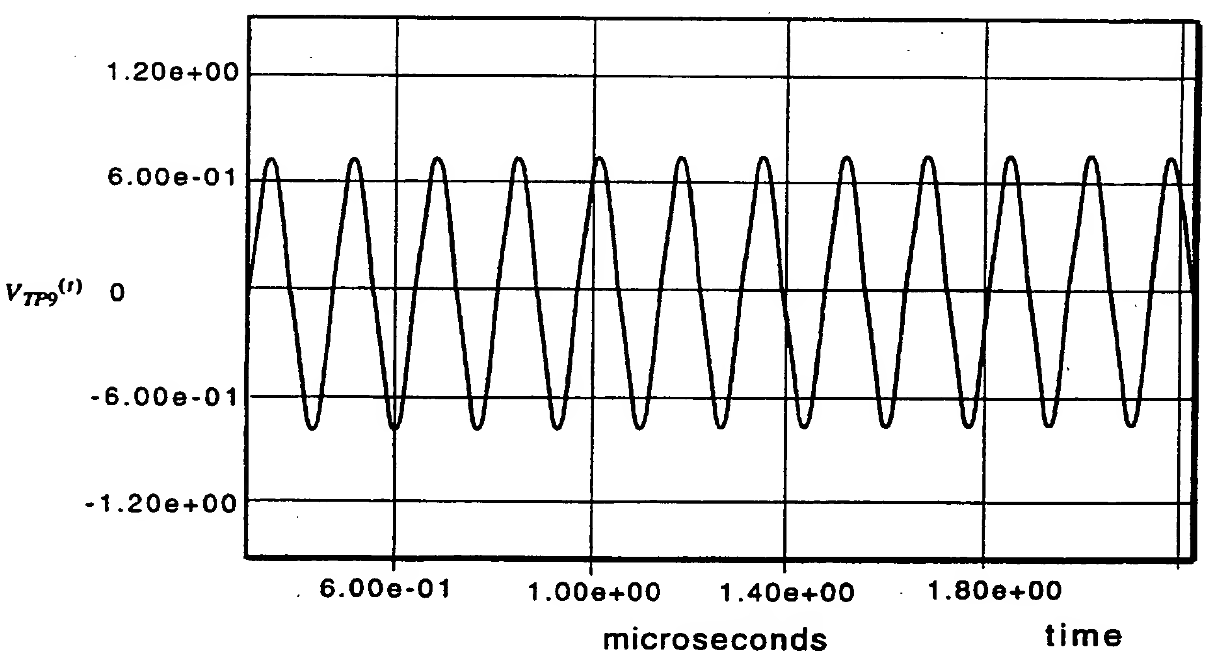


FIGURE 8D



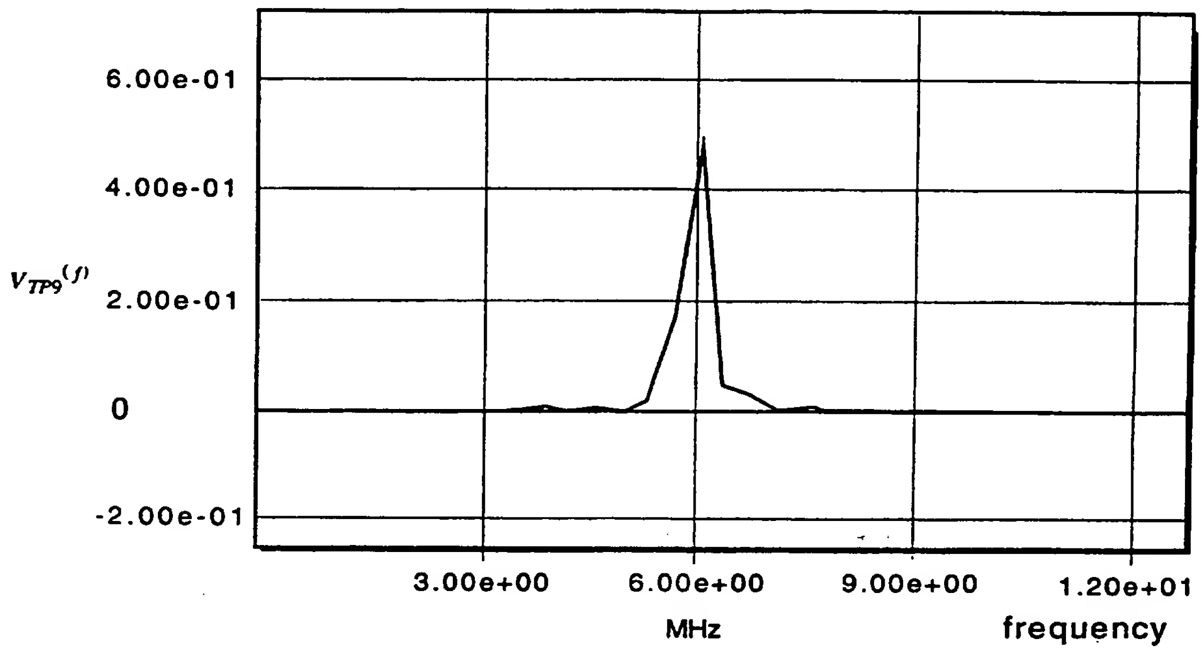
$f_s = 24$ MHz, $f_{in} = 114$ MHz, $f_{OUT} = 6$ MHz, τ track ,7ns

FIGURE 8E



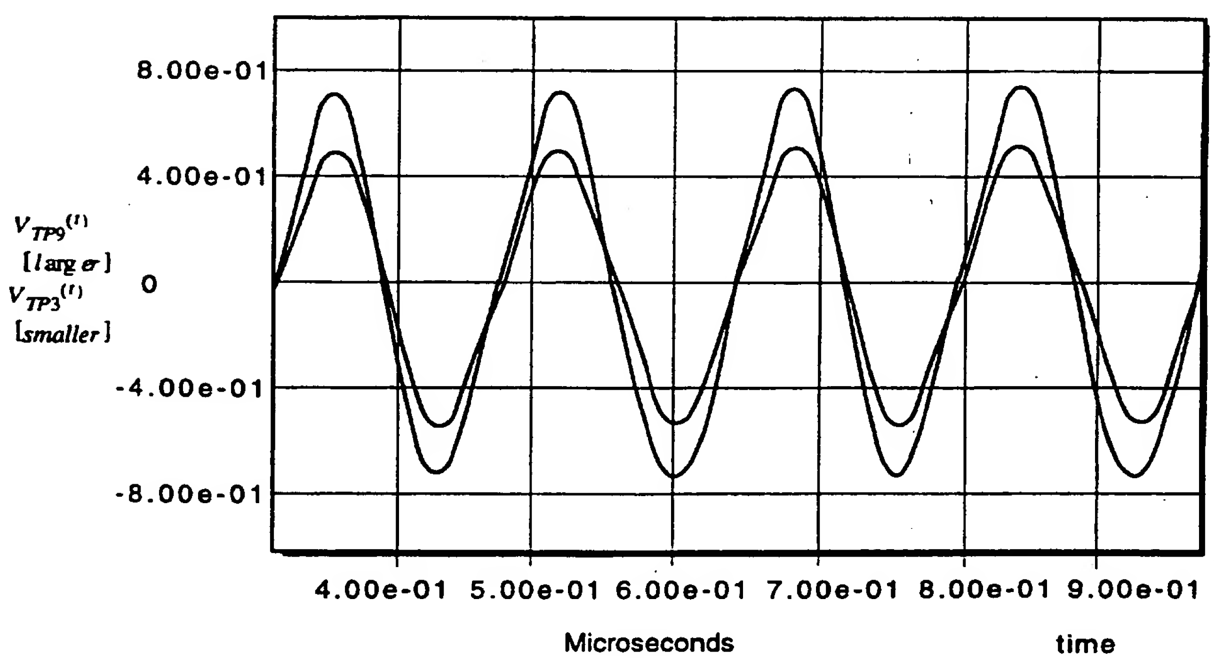
$f_s = 24E6$, $f_{in} = 114$ MHz, $f_{OUT} = 6$ MHz, τ track $= 7ns$

FIGURE 8F



$f_s = 24\,E6, f_{in} = 114\ MHz, f_{OUT} = 6\,MHz, \tau\ track = 7ns$

FIGURE 8G



$STDMIXER: 114\ MHz \times 120\,MHz \rightarrow 6\,MHz\,(AMP\ . = \frac{1}{2})$

$T/_M\ MIXER\ f_s = 24\,MHz, f_{in} = 114\,MHz \rightarrow 6\,MHz\,(AMPL\,0.74)$

FIGURE 9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/08233

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : H04B 1/26
US CL :455/313, 327/553
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 455/313, 333: 327/551-559, 91, 94, 113; 329/318, 320, 341, 361; 375/224; 328/127; 341/123, 61; 330/9; 364/572, 724.01

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

APS

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

none

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US, A, 5,339,459 (SCHILTZ ET AL) 16 August 1994 (see figure 1, col.1, lines 50-57 and col. 2, lines 30-37)	1-5
Y	US, A, 5,050,474 (OGAWA ET AL) 24 September 1991 (see figure 3 and col. 8, lines 50-57)	1-5
A	US, A, 4,673,916 (KITAMURA ET AL) 16 June 1987	1-5
A	US, A, 4,990,911 (FUJITA ET AL) 05 February 1991	1-5
A	US, A, 4,893,088 (MYERS ET AL) 09 January 1990	1-5
A	US, A, 3,573,626 (ERTMAN) 06 April 1971	1-5

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

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"E" earlier document published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

29 AUGUST 1995

Date of mailing of the international search report

05 OCT 1995

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